*Coding Standards*

1. The project is to be implemented in SystemVerilog Hardware Description Language.
2. Heading of all source files should include a file name, module description and top-level context.
3. File names
   1. All file names will be prefixed with rtc\_.
   2. File names will be the same as the module entity name.
   3. File names should only use lower-case characters.
   4. Ports and signals:
   5. Ports and signals shall have their names present in code with all lower-case characters.
   6. Upper-case characters are reserved for parameter variables and constants.
   7. Should not use inout ports.
   8. Use “i\_” prefix for input ports.
   9. Use “o\_” prefix for output ports.
   10. For active-low signals, the signal name shall be appended with “\_n” postfix.
   11. For port declarations, add comment with port’s usage/function in the module.
   12. Limit of one port or signal declaration per line.
4. Processes and Sequential Statements
   1. Include a comment that describes the process or statement functionality.
   2. All processes should include a tag that serves as a short summary of its function.
   3. Provide spaces between statement declarations and sensitivity lists.
   4. Sensitivity lists should not include complex logical functions.
   5. Sensitivity list of a synchronous process only includes reset and clock two signals.
   6. Each clock signal shall have "clk" designation as part of its name
   7. Active low reset.
5. Maximum of one module per file (module or a testbench, not both).
6. Usage of “tab” character(‘\t’) in code files is prohibited, use 4 ’spaces’ instead.
7. Types and subtypes uses a \_t suffix
8. Vector ranges
   1. Use descending [N:0] as default range
   2. Only use ascending ([0:N] when describing the depth of a memory array